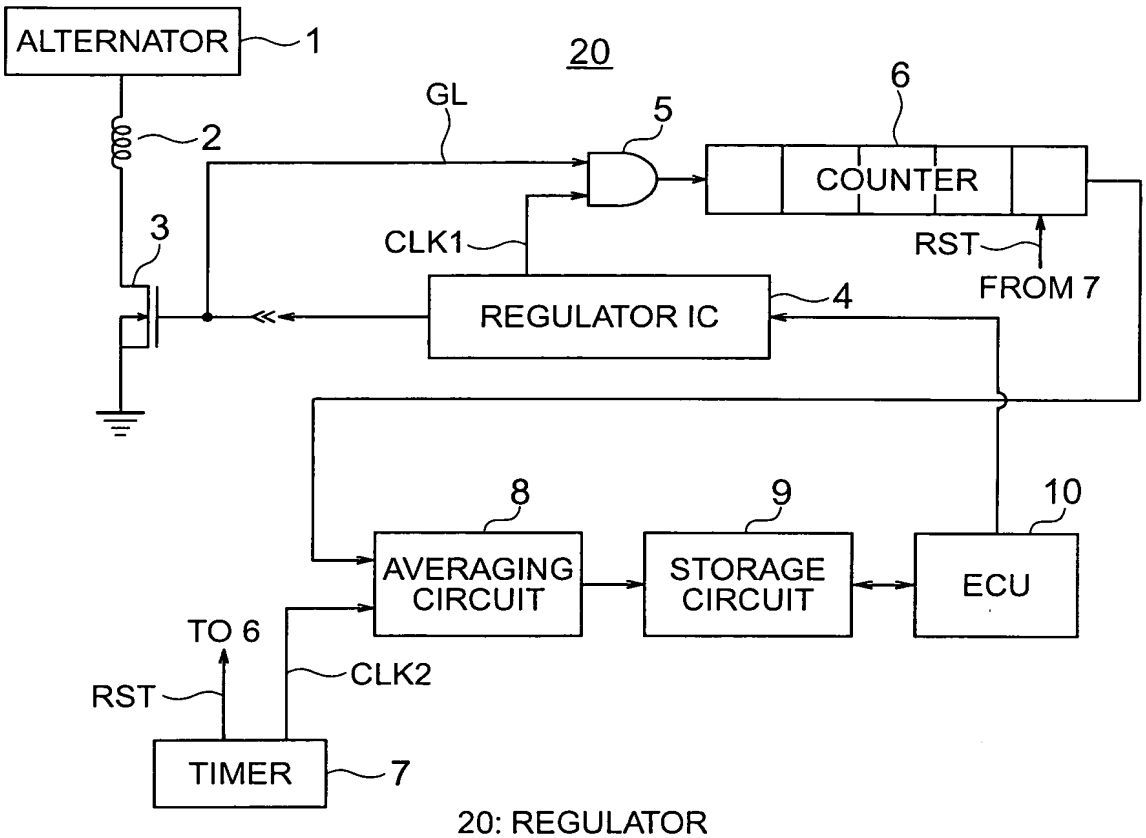
FIG. 1



20: REGULATOR
CLK2: SAMPLING SIGNAL
GL: GATE LOGIC SIGNAL
RST: RESET SIGNAL

FIG. 2

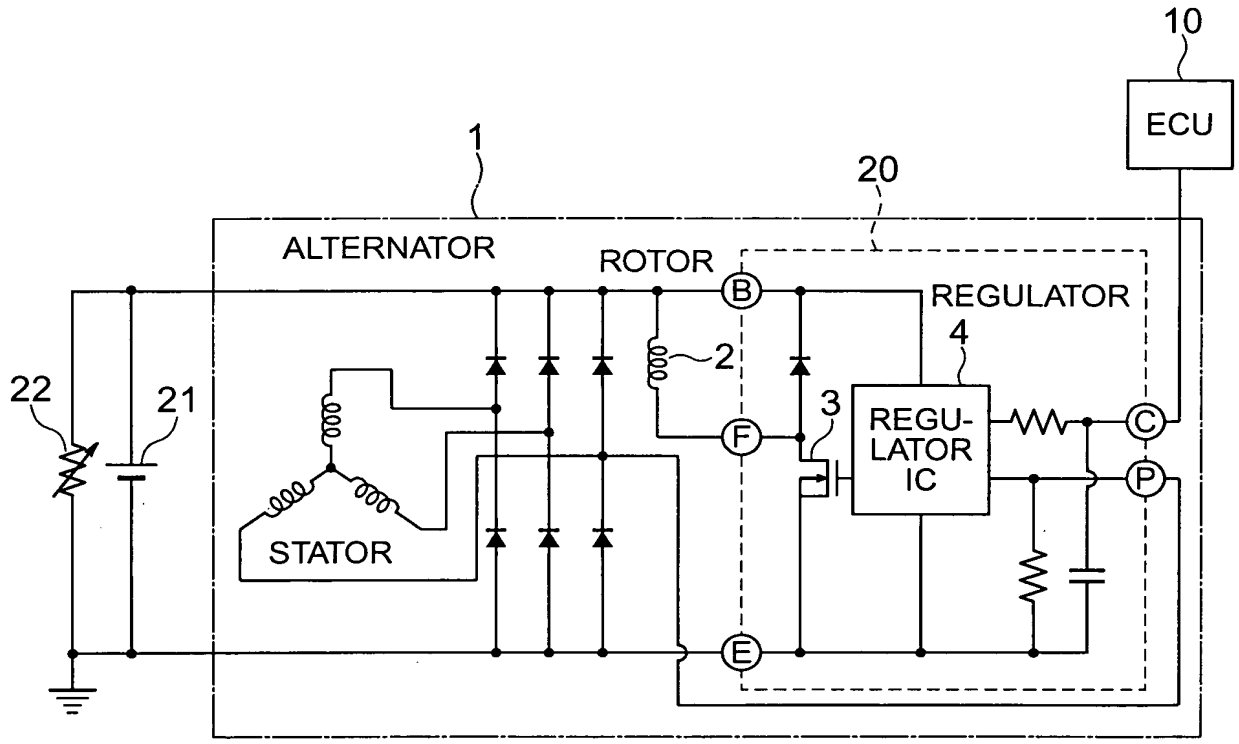


FIG. 3

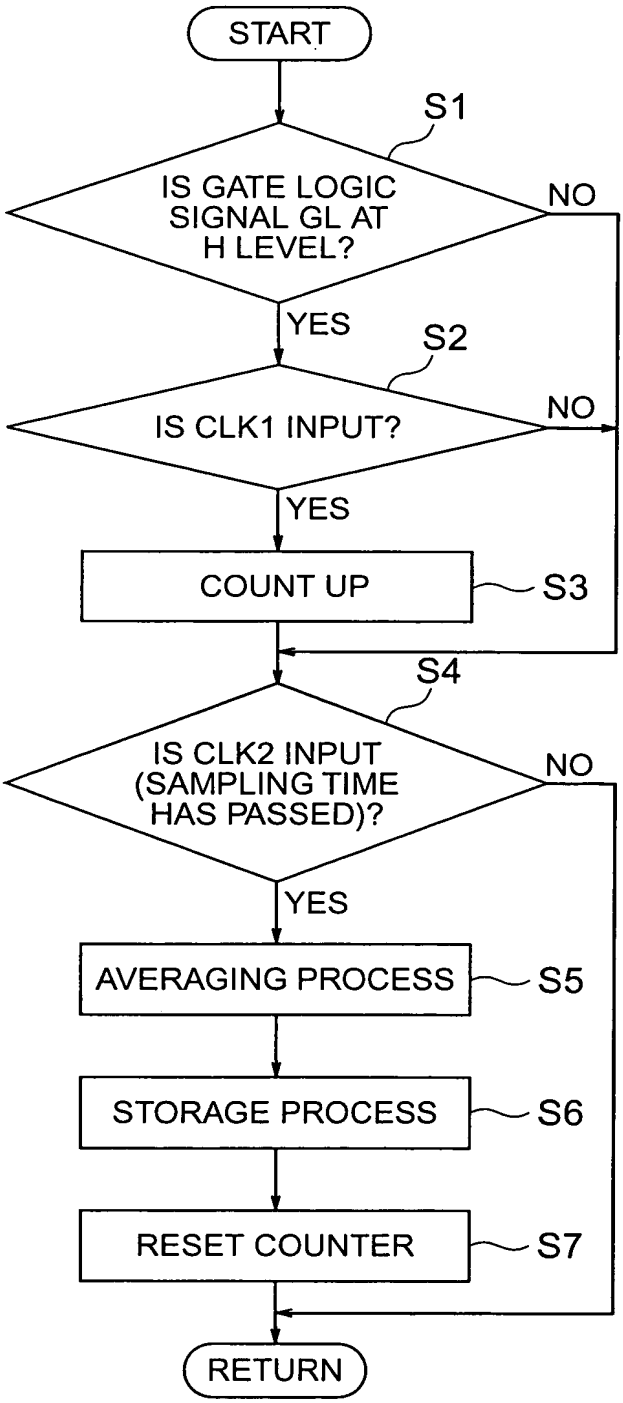
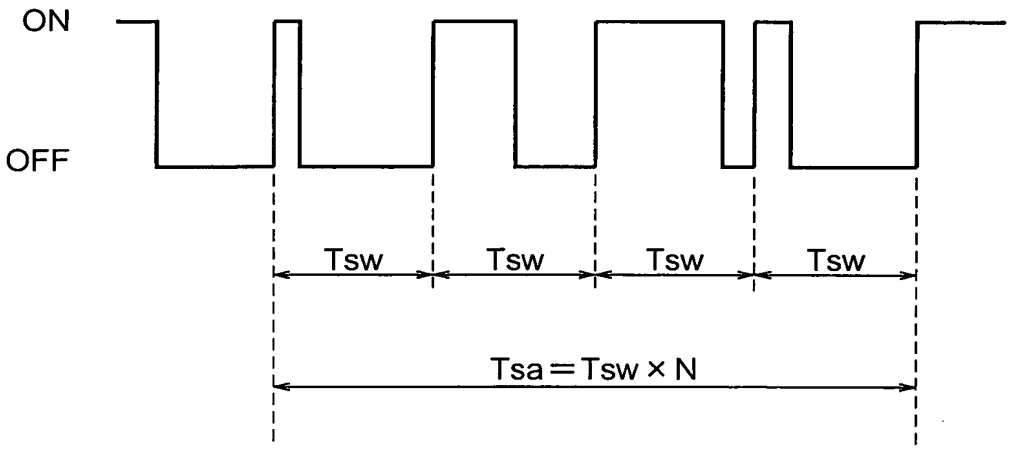
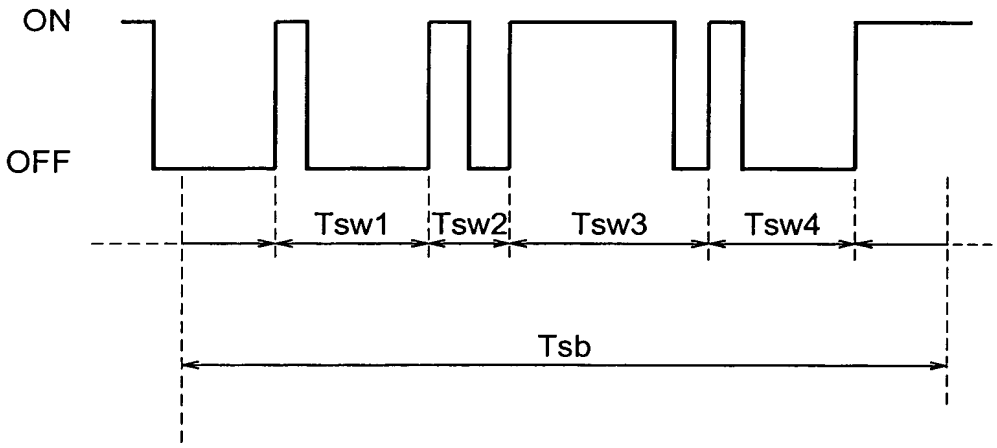

START
S1
IS GATE LOGIC SIGNAL GL AT H LEVEL?
NO
YES
S2
IS CLK1 INPUT?
NO
YES
COUNT UP
S3
S4
IS CLK2 INPUT (SAMPLING TIME HAS PASSED)?
NO
YES
AVERAGING PROCESS
S5
STORAGE PROCESS
S6
RESET COUNTER
S7
RETURN

FIG. 4



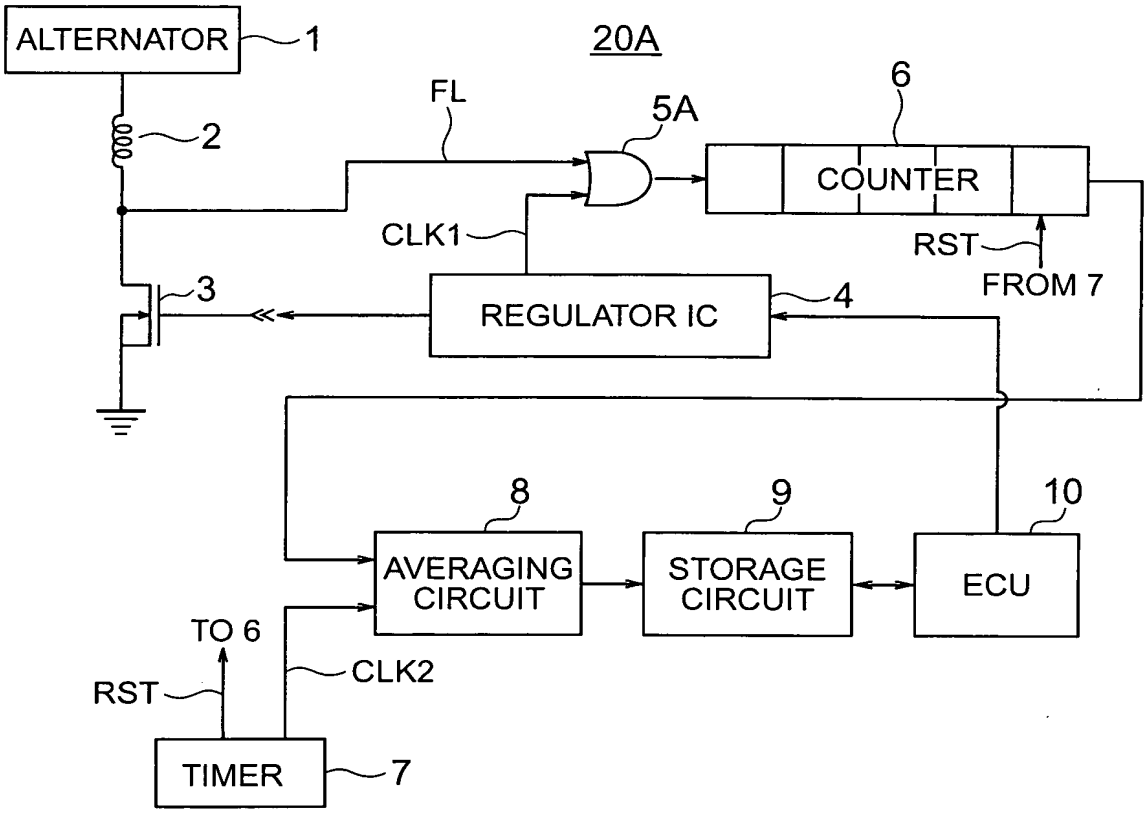
Tsw: FIELD SWITCH CYCLE
TSa: SAMPLING CYCLE

FIG. 5



Tsw 1 to Tsw4: FIELD SWITCH CYCLE
TSb: SAMPLING CYCLE

FIG. 6



FL: FIELD LOGIC SIGNAL